We claim:

1. An optoelectronic package comprising:

a base chip, the chip comprising a base chip V-groove;

a fiber array, the array comprising an array V-groove formed in a rear portion and a front portion of the array;

a first wick stop disposed between the rear and front portions; and

an optical fiber, having an angled endface, disposed in both V-grooves to substantially couple the chip and array.

2. The optoelectronic package as in claim 1 wherein the array further comprises a sealing lid.

3. The optoelectronic package as in claim 2 wherein the sealing lid comprises a monolithic sealing lid.

4. The optoelectronic package as in claim 1 wherein the base chip further comprises an etch stop layer under the laser.

5. The optoelectronic package as in claim 4 wherein the layer comprises SiO_2.

6. The optoelectronic package as in claim 4 wherein the layer comprises silicon nitrate.

7. The optoelectronic package as in claim 4 wherein the layer comprises AL_2O_3.

8. The optoelectronic package as in claim 1 wherein the array comprises a first pit and the chip comprises a second pit.

9. The optoelectronic package as in claim 1 further comprising an alignment sphere, wherein the sphere is disposed between the first and second pits.

10. The optoelectronic package as in claim 1 wherein the array comprises a middle portion bordered by the first wick stop and a second wick stop.

11. The optoelectronic package as in claim 1 wherein the base chip further comprises a surface device.

12. The optoelectronic package as in claim 11 wherein the surface device comprises a VCSEL.

13. The optoelectronic package as in claim 11 wherein the surface device comprises a photodetector.

14. A method for coupling optoelectronic packages comprising:

forming a base chip V-groove in a base chip;

forming an array V-groove in a rear portion and a front portion of a fiber array;

disposing a first wick stop between the rear and front portions; and

disposing an optical fiber, having an angled endface, in both V-grooves to substantially couple the chip and array.

15. The method as in claim 14 further comprising disposing a surface device on the base chip.

16. The method as in claim 15 wherein the surface device comprises a VCSEL.

17. The method as in claim 15 wherein the surface device comprises a photodetector.

18. The method as in claim 14 further comprising enclosing the surface device with a sealing lid.

19. The method as in claim 18 wherein the sealing lid comprises a monolithic sealing lid.

20. The method as in claim 14 further comprising forming an etch stop layer in the base chip.

21. The method as in claim 20 wherein the layer comprises SiO_2.

22. The method as in claim 20 wherein the layer comprises silicon nitrate.

23. The method as in claim 20 wherein the layer comprises AL_2O_3.

24. The method as in claim 14 further comprising forming a first pit on the array and a second pit on the base chip.

25. The method as in claim 24 further comprising disposing an alignment sphere between the first and second pits.

26. The method as in claim 14 further comprising forming a middle portion bordered by the first wick stop and a second wick stop.